

1/18  
 Tomooka et al  
 JP4-1999-0267051(8728-457)(MU)

FIG. 1

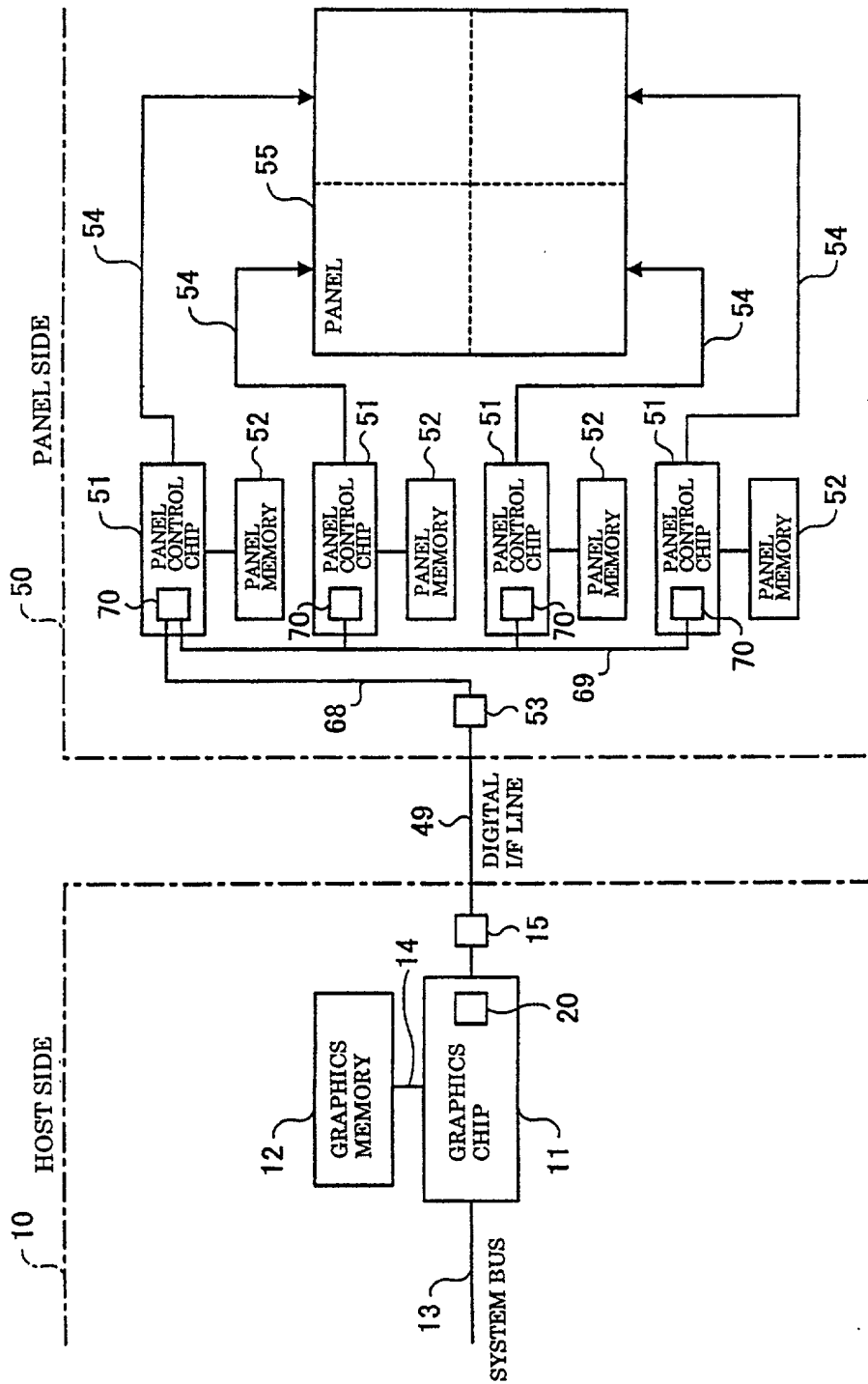


FIG. 2

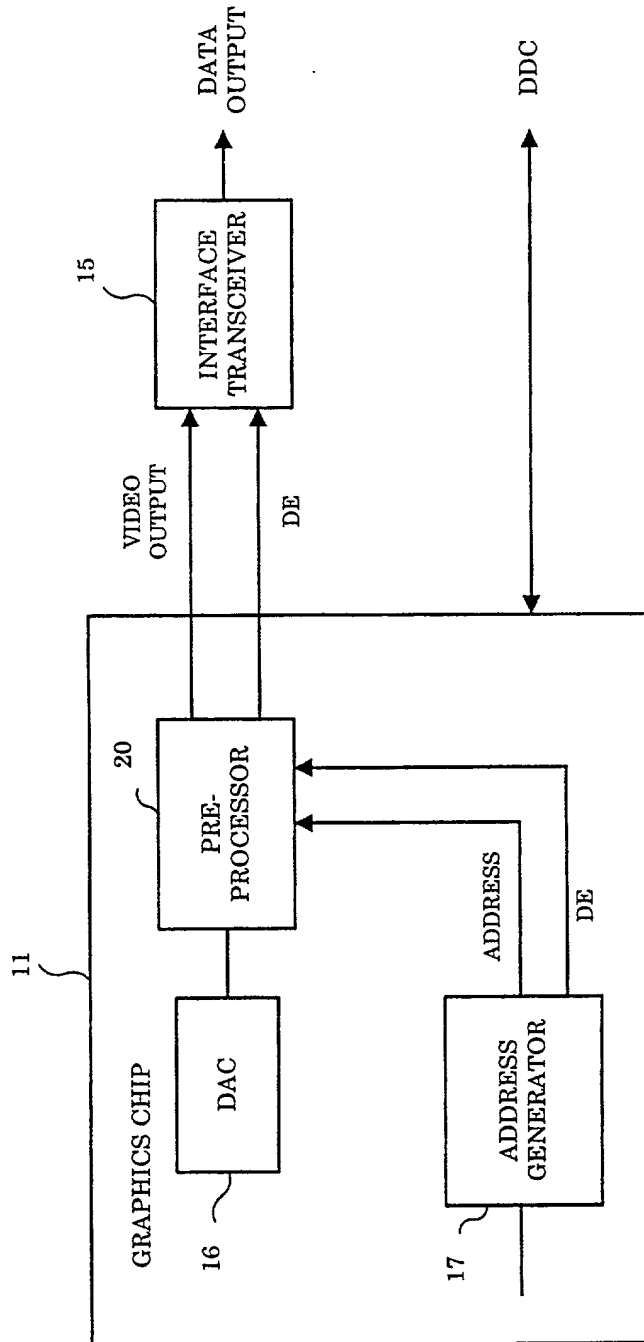
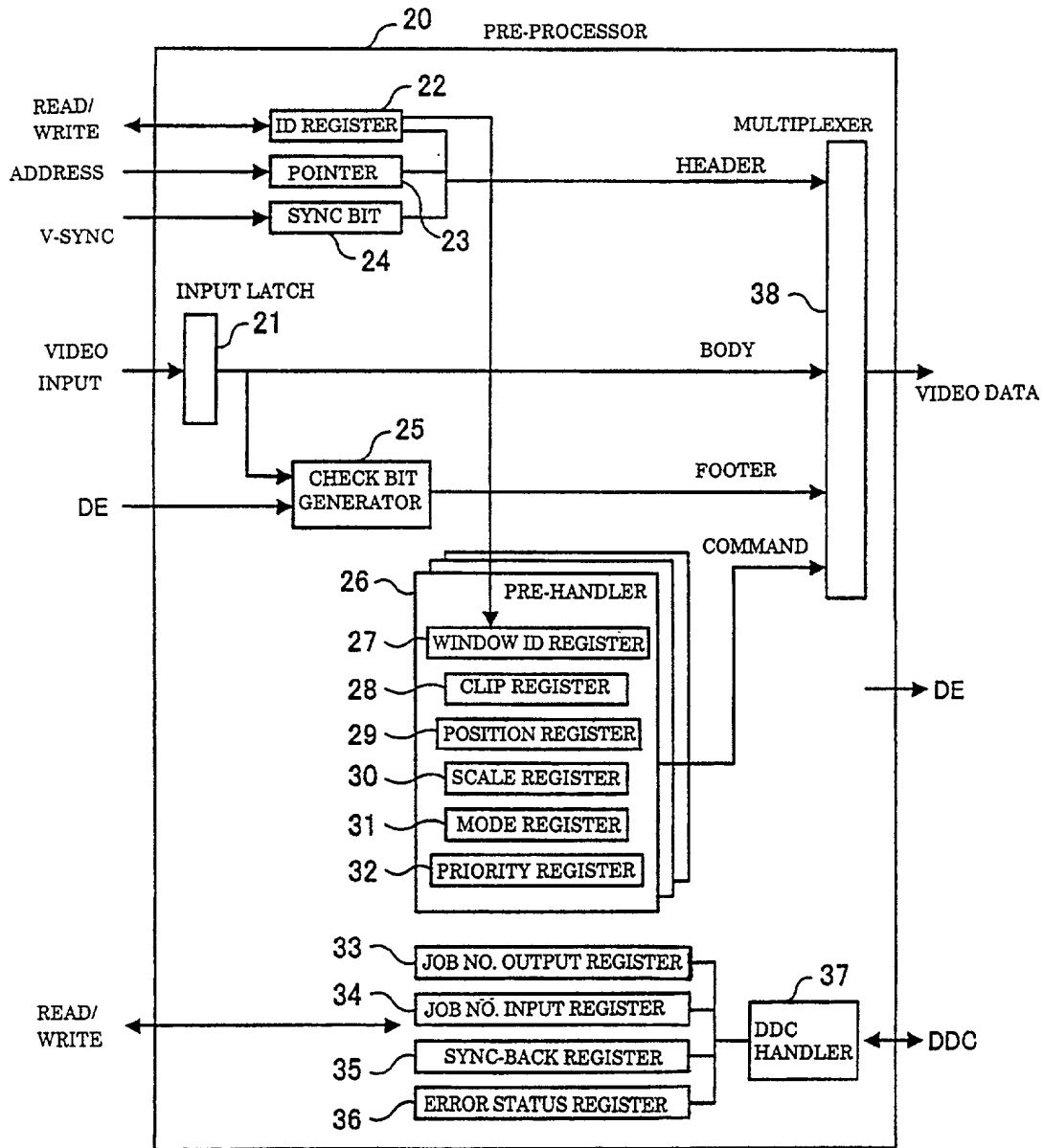


FIG. 3



4/18  
JP9-1999-0267 US1(8928457)

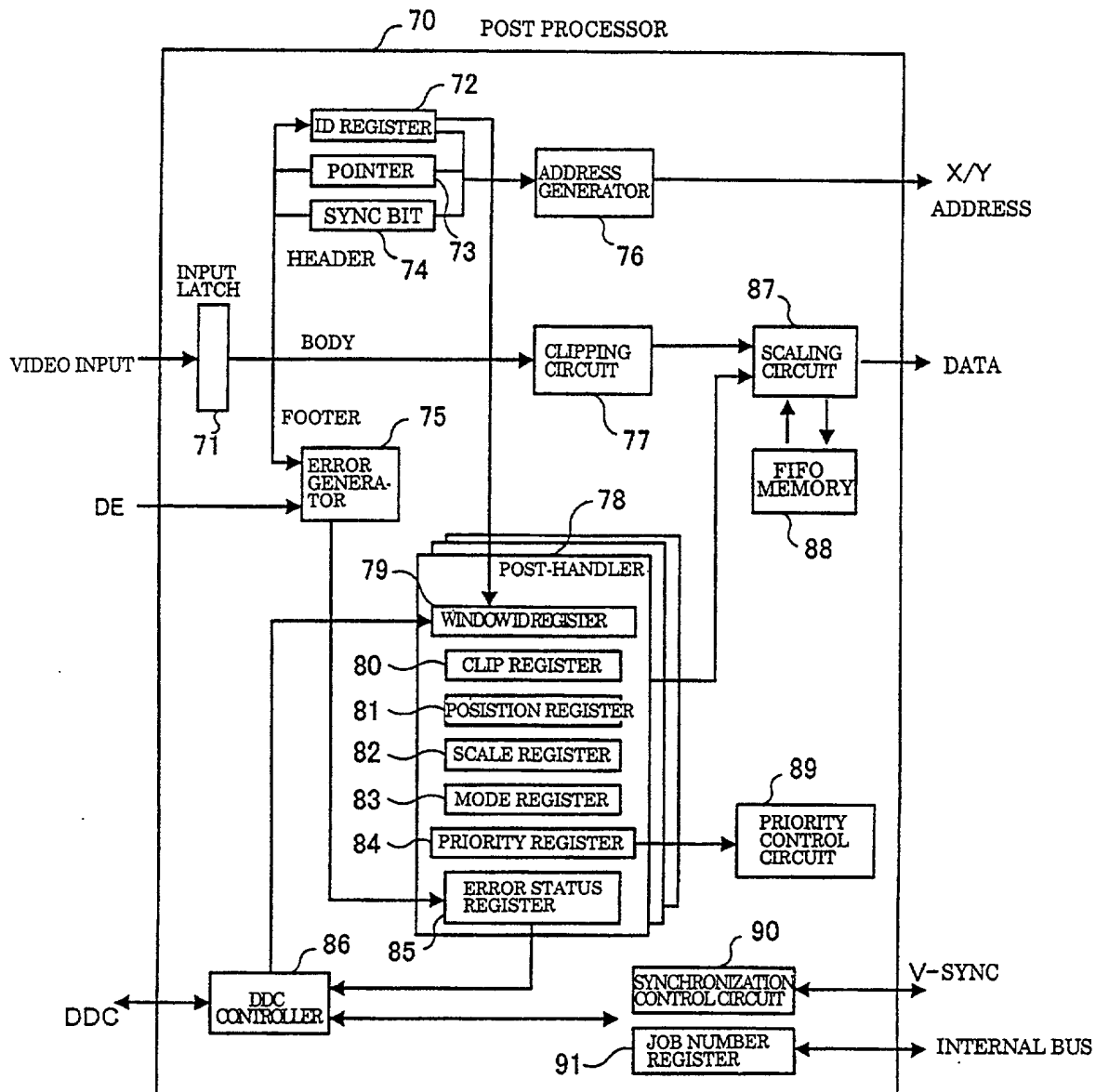
FIG. 4

## VIDEO OUTPUT

H/V SYNCHRONIZED  
SIGNAL

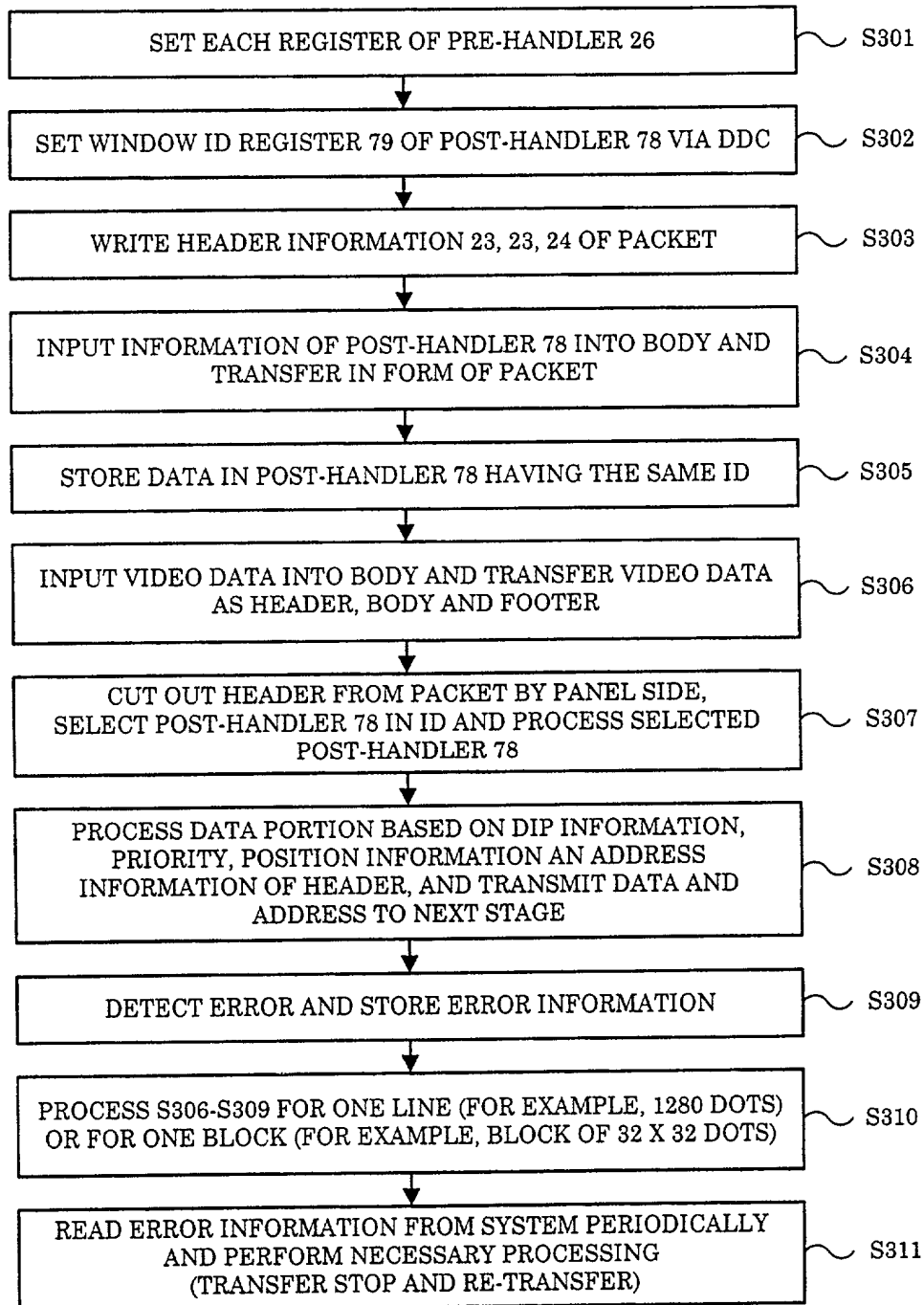
5/18  
JP9-1999-0267251(8728-457)

FIG. 5



6/18  
JP9-1999-0267051(8728457)

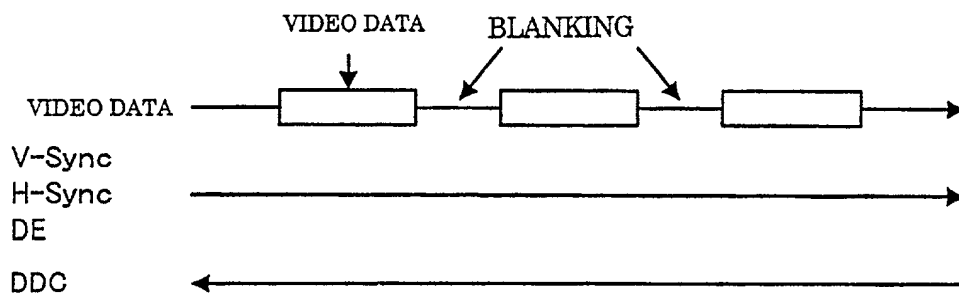
FIG. 6



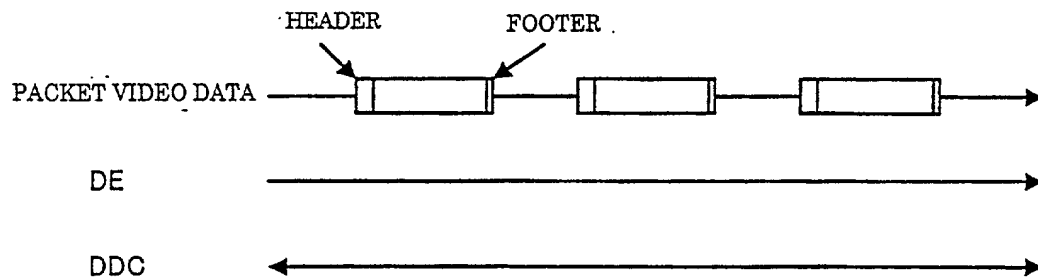
00627"6452250

Variable	Mean	SD	Min	Max	Skewness	Kurtosis	Normality
Age	35.2	12.5	18	65	0.15	-0.5	0.98
Gender	0.5	0.5	0	1	0.0	0.0	0.99
Marital Status	0.7	0.5	0	1	0.0	0.0	0.99
Education	12.5	2.5	9	16	0.1	-0.2	0.97
Income	1500	500	500	3000	0.2	-0.1	0.96
Health	0.8	0.4	0	1	0.0	0.0	0.99
Stress	4.5	1.5	1	7	0.1	-0.3	0.98
Depression	2.5	1.0	1	5	0.1	-0.2	0.97
Life Satisfaction	5.5	1.0	1	7	0.1	-0.3	0.98
Resilience	4.0	1.5	1	7	0.1	-0.2	0.97
Optimism	5.0	1.0	1	7	0.1	-0.2	0.98
Self-Esteem	4.5	1.0	1	7	0.1	-0.2	0.97
Emotional Stability	5.0	1.0	1	7	0.1	-0.2	0.98
Life Satisfaction	5.5	1.0	1	7	0.1	-0.3	0.98
Resilience	4.0	1.5	1	7	0.1	-0.2	0.97
Optimism	5.0	1.0	1	7	0.1	-0.2	0.98
Self-Esteem	4.5	1.0	1	7	0.1	-0.2	0.97
Emotional Stability	5.0	1.0	1	7	0.1	-0.2	0.98

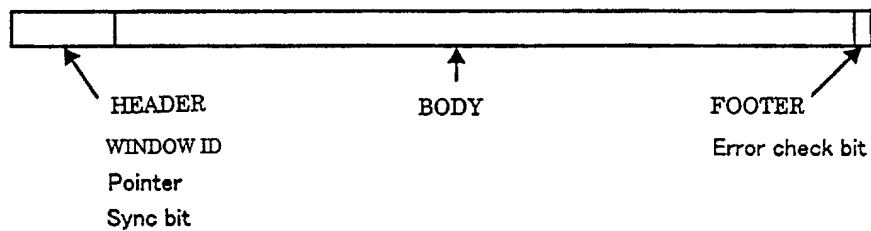
FIG. 7



(a) CONVENTIONAL TRANSFER OF VIDEO DATA



### (b) TRANSFER OF VIDEO DATA IN THIS EMBODIMENT



### (c) FORMAT OF PACKET VIDEO DATA

8/18  
JP9-1999-0267051(8728-457)

FIG. 8

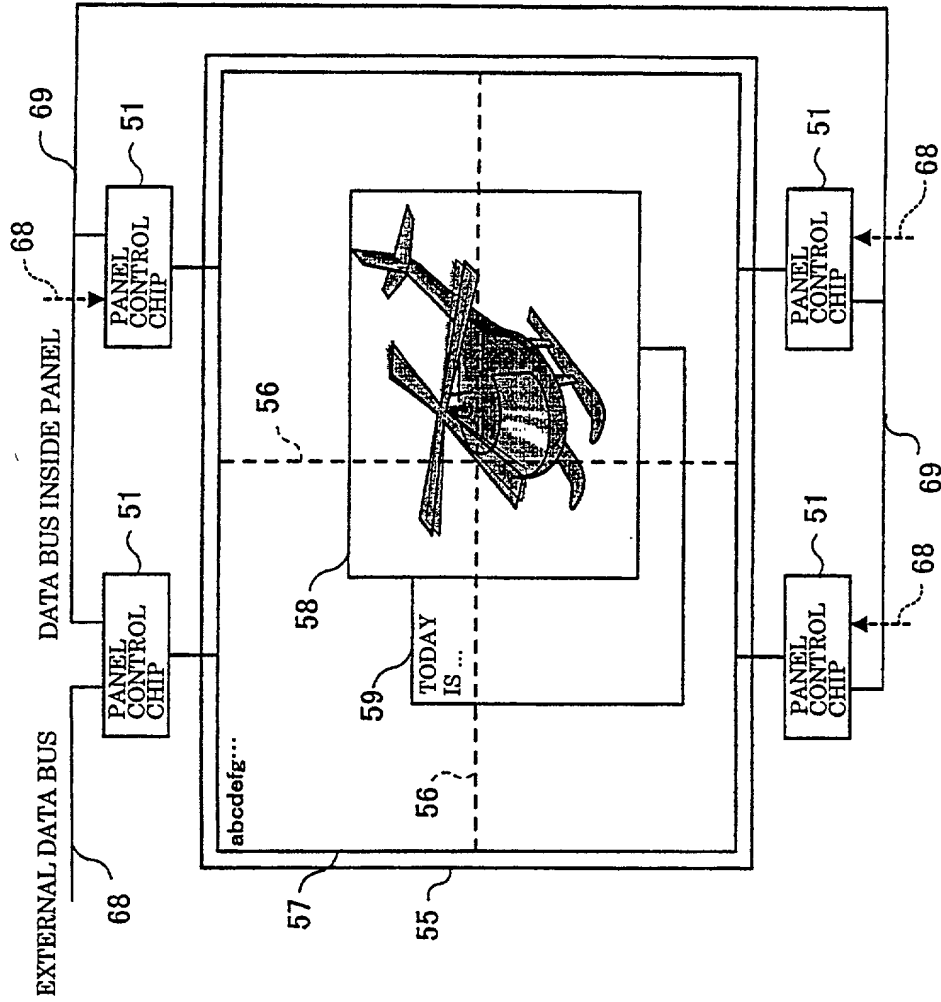
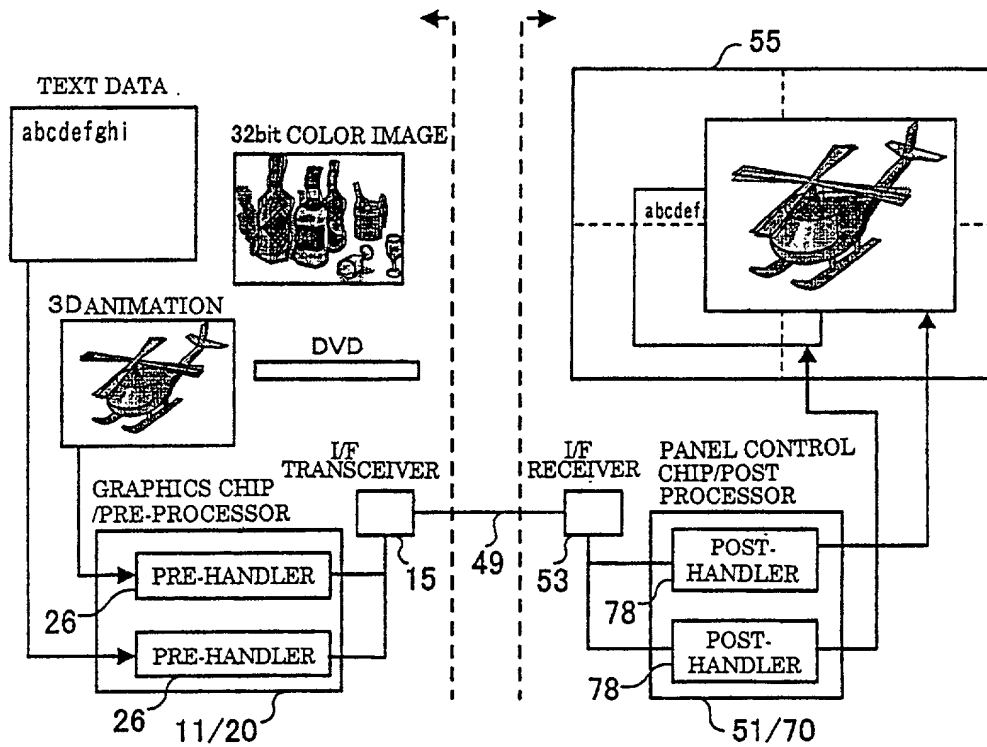
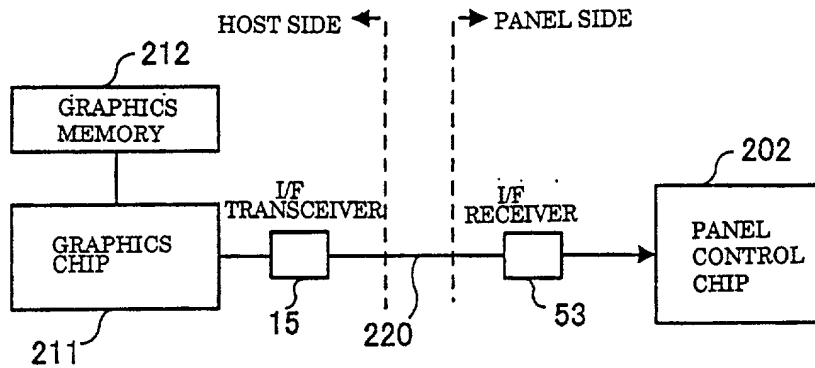


FIG. 9



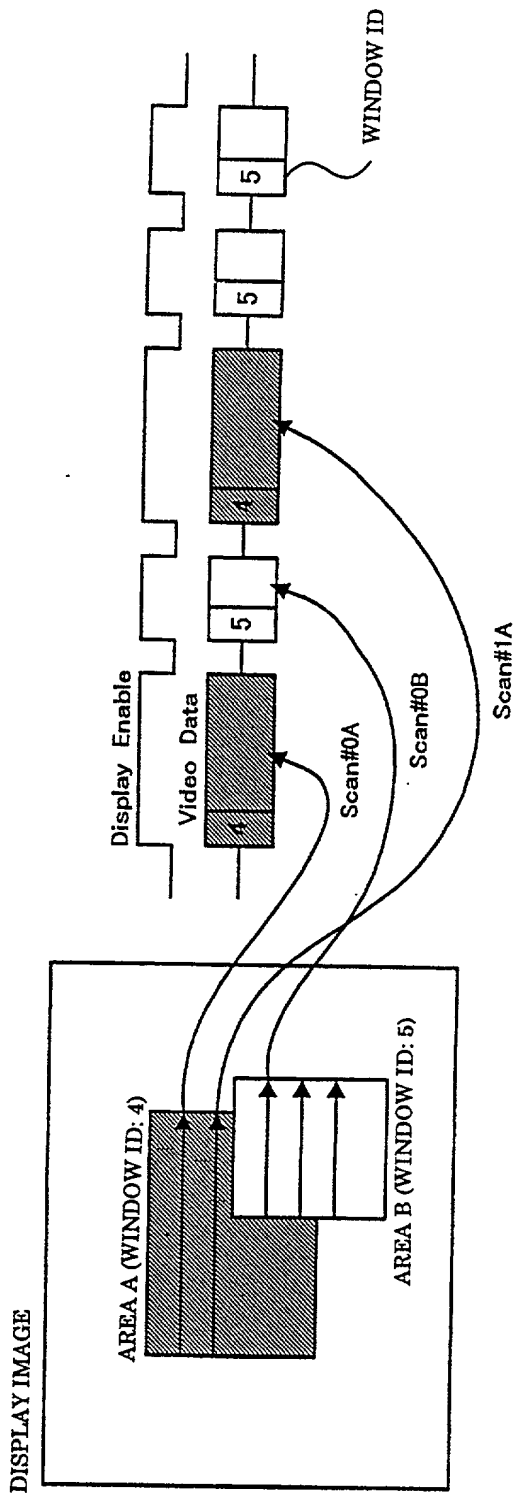
(a) DATA SOURCE AND PROCESSING SYSTEM



(b) LIMITATION OF DATA BAND WIDTH

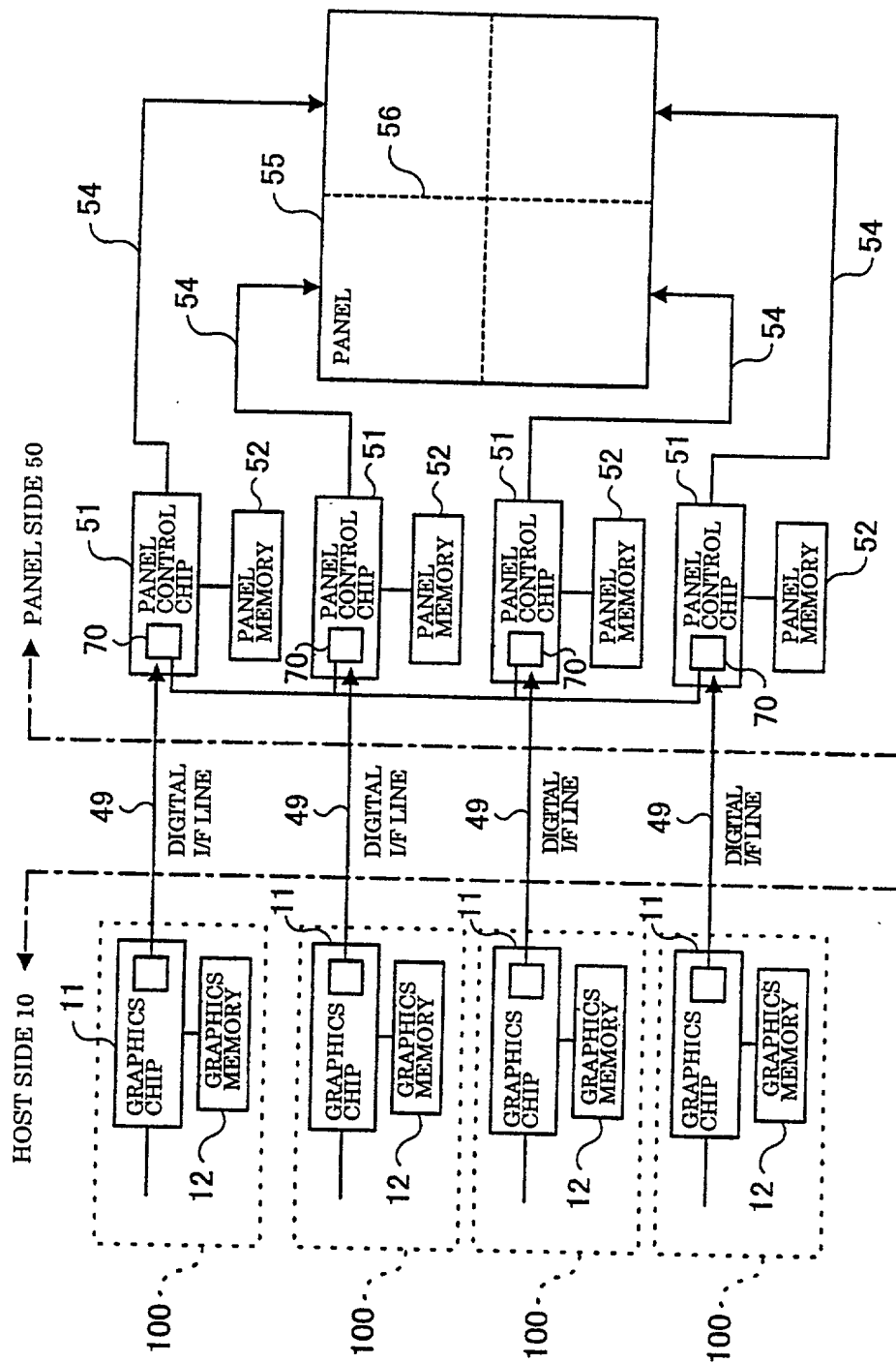
19/18  
JP9-1999-0267051(8928-457)

FIG. 10



11/18  
JP9-1999-0267251(8728-457)

FIG. 11



Parameter	Unit	Value
Temperature	°C	25.0
Pressure	atm	1.0
Flow rate	L/min	1.0
Sample concentration	mg/mL	1.0
Sample volume	μL	1.0
Injection volume	μL	1.0
Column	μm	5.0
Mobile phase		
A		
B		
Gradient		
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The diagram illustrates a dual-channel video system architecture, divided into two main sections: **HOST SIDE 10** and **PANEL SIDE 50**.

**HOST SIDE 10 (Left):**

- GRAPHICS CHIP/PRE-PROCESSOR (11/20):** Contains a **SYNCHRONIZATION CONTROL CIRCUIT (43)** which includes an **OFFSET REGISTER (41)**, an **ADDER (42)**, a **MULTIPLEXER (43)**, and a **VERTICAL SYNCHRONIZATION COUNTER (44)**.
- DDC HANDLER (37):** Receives **H-Sync** and **DDC** signals. It is connected to **JOB NO. OUTPUT REGISTER (33)** and **JOB NO. INPUT REGISTER (34)**.
- READWRIT CONTROL (45):** Receives a signal **to CPU** and is connected to the **JOB NO. OUTPUT REGISTER (33)**.

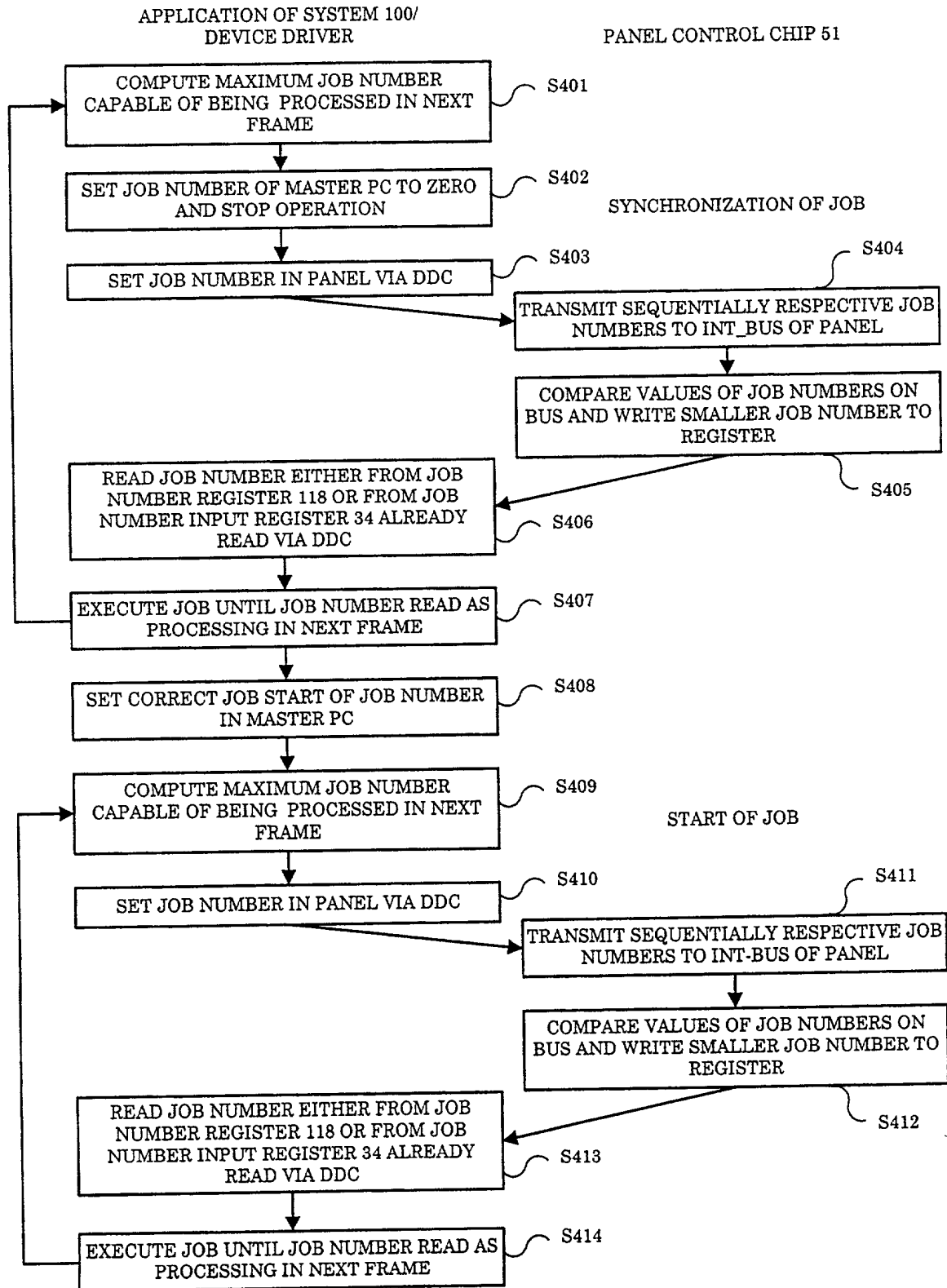
**PANEL SIDE 50 (Right):**

- PANEL CONTROL CHIP/POST-PROCESSOR (51/70):** Contains a **SYNCHRONIZATION CONTROL CIRCUIT (114)** which includes an **OFFSET REGISTER (113)**, an **ADDER (114)**, and a **VERTICAL SYNCHRONIZATION COUNTER (112)**.
- DDC HANDLER (115):** Receives **DDC** and **INT\_HS/INT\_VSYNC** signals. It is connected to **JOB NO. INPUT REGISTER (117)** and **JOB NO. OUTPUT REGISTER (118)**.
- COMPARATOR (119):** Receives signals from the **JOB NO. INPUT REGISTER (117)** and **JOB NO. OUTPUT REGISTER (118)**.
- INTERNAL BUS CONTROLLER (120):** Connected to the **COMPARATOR (119)** and the **INT BUS (121)**.

**Interconnections:**

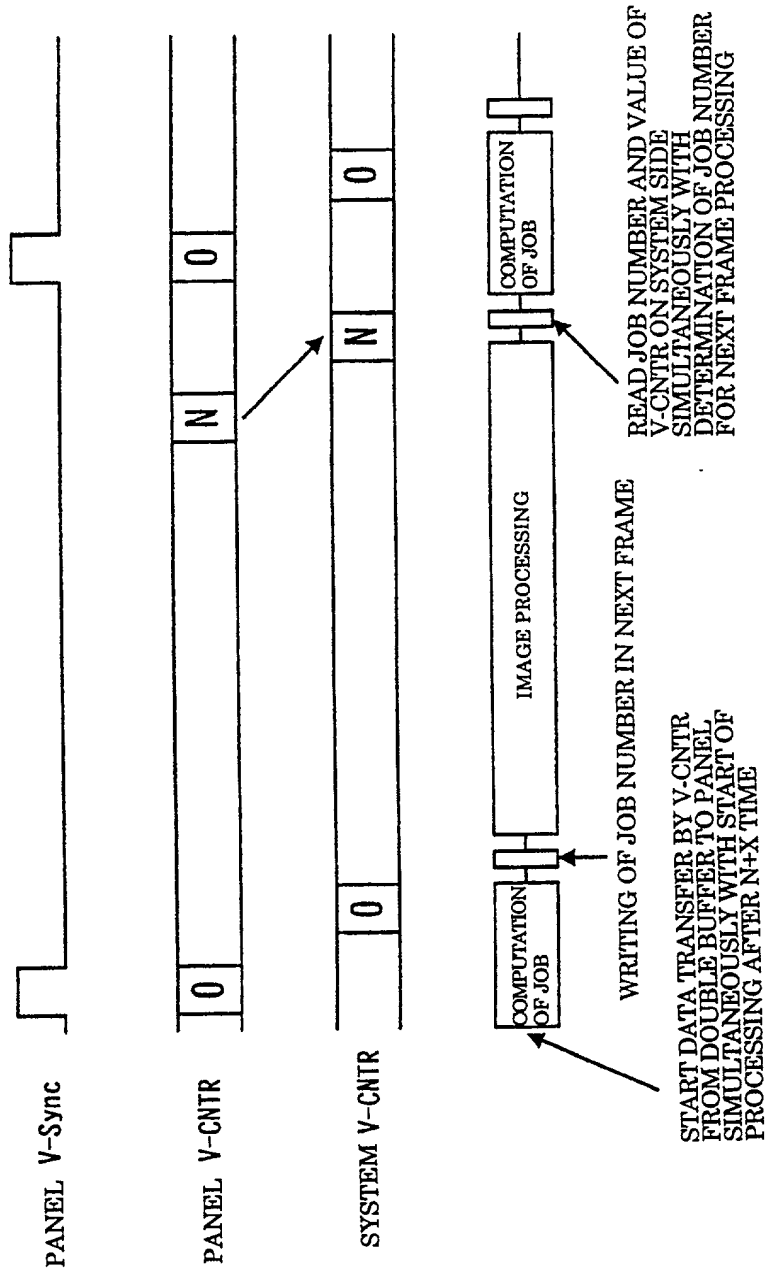
- DDC (Data Display Channel):** A bidirectional bus connecting the **DDC HANDLER (37)** on the Host Side to the **DDC HANDLER (115)** on the Panel Side.
- INT\_HS/INT\_VSYNC:** Signals from the Host Side to the Panel Side.
- INT BUS (121):** An internal bus connecting the **INTERNAL BUS CONTROLLER (120)** to the **INT\_HS/INT\_VSYNC** inputs.

FIG. 13



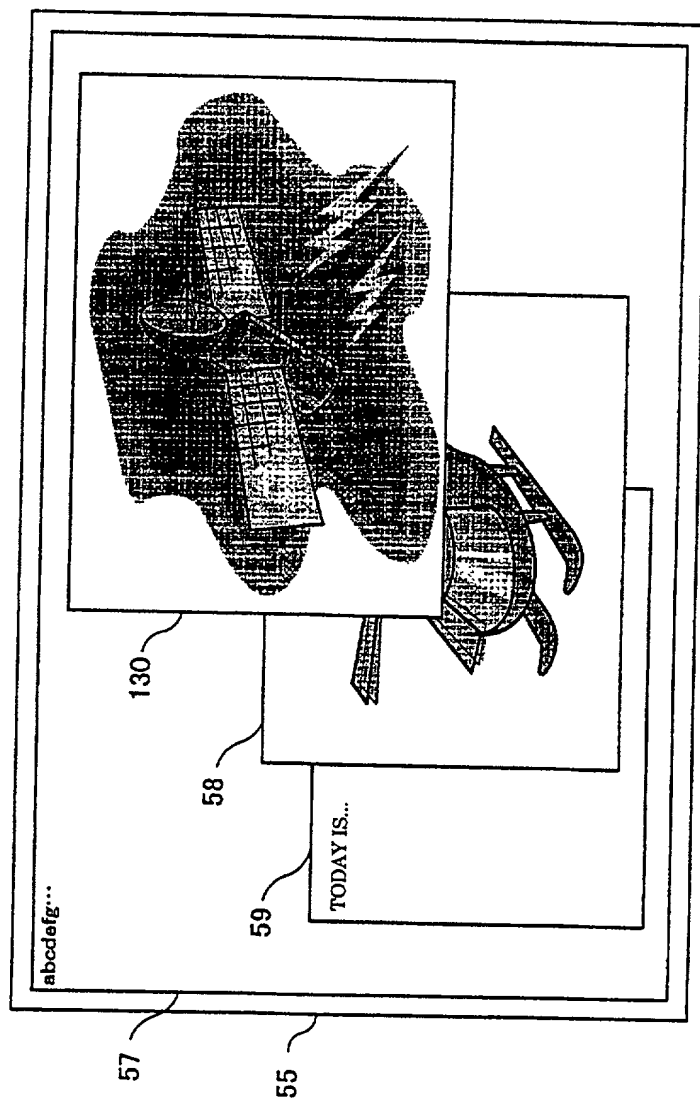
14/18  
JP9-1999-0267051(8728-457)

FIG. 14



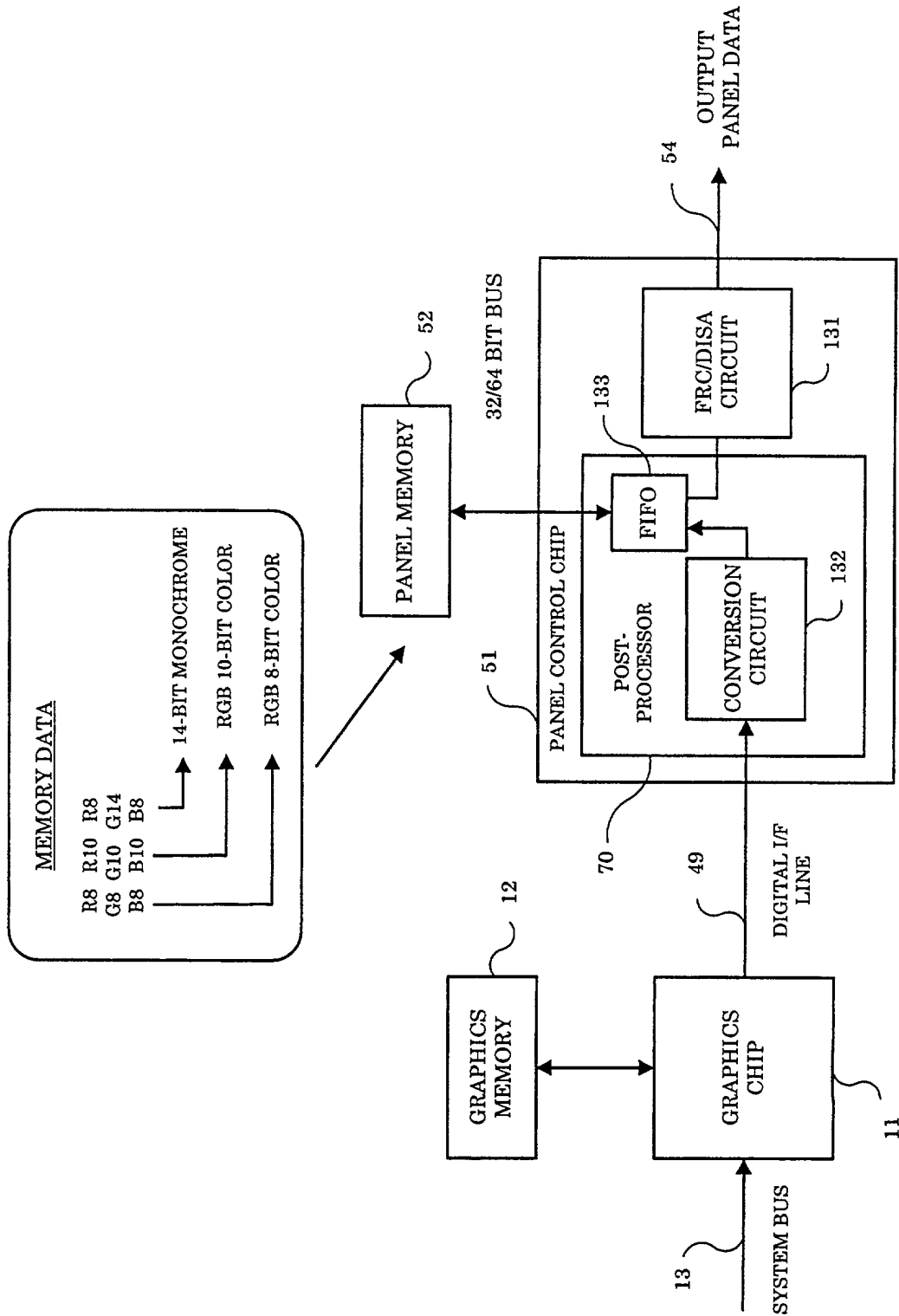
15/18  
JP9-1999-0267051(8728-457)

FIG. 15



16/18  
JP9-1999-0267US1(8728-457)

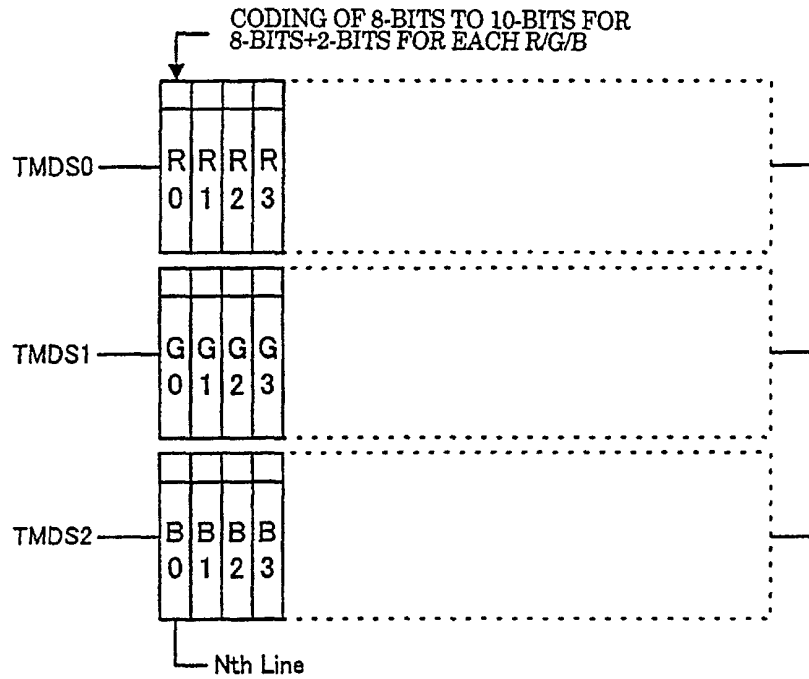
FIG. 16



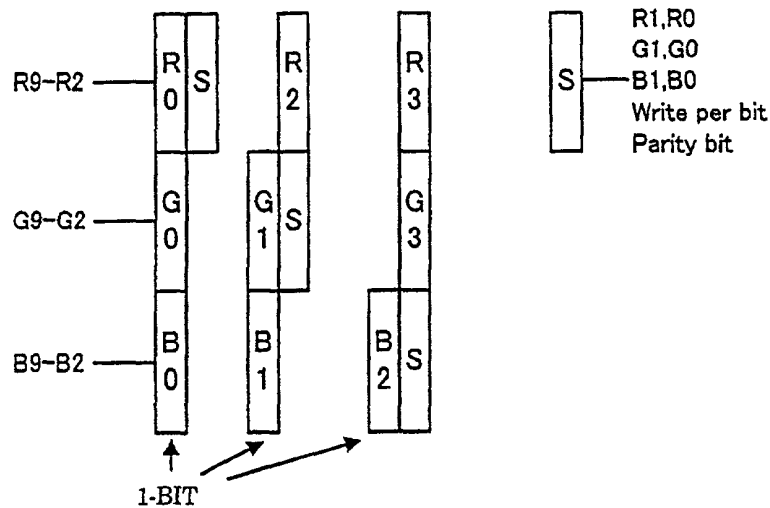
17/18

JP9-1999-0267051(8728-457)

FIG. 17



(a) TMDS DATA TRANSFER



(b) BIT ASSIGN OF 30-BIT COLOR

18/18  
JP9-1999-026705(8728457)

FIG. 18

